Abstract

A supplemental capacitor is formed using the large capacitance between the wirings (M11 and M12) and that between the through-holes (B11 and B12) because of downsizing of the process technique. The inter-wiring capacitor and inter-through-hole capacitor can be arranged at any optional position within the semiconductor device. The supplemental capacitor can be easily formed in the vicinity of the area where switching noise is generated, thereby effectively realizing the countermeasure for power source noise. In the process technique with advanced downsizing, a capacitor having large capacitance can be formed with a smaller area. In addition, the capacitor can be formed in the same process as the other device such as a transistor without adding any special step.